

EAST Search History

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|-------|-------|--|---|------------------|---------|------------------|
| L1 | 2632 | (memory same attribut\$3) and configur\$3 and logical and interconnect\$3 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |
| L2 | 2 | (memory same component same attribut\$3) and interface and implement\$6 and specification and topology and interconnect\$4 and messag\$3 and generat\$3 and configur\$4 and "716"/\$.ccls. | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |
| L3 | 15 | (FPGA or (programmable adj logic adj design) same implement\$5) and (memory same attribut\$3) and configur\$3 and logical and interconnect\$3 and topology and "716"/\$.ccls. | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |
| L4 | 104 | (FPGA or CLB or PLD or (programmable adj logic adj design)) and (memory same attribut\$3) and configur\$3 and logical and interconnect\$3 and topology and component and architecture and implement\$5 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |
| L5 | 0 | ((memory same component same attribut\$3) and interface and implement\$6 and specification and topology and interconnect\$4 and messag\$3 and generat\$3 and configur\$4 and logic\$4).CLM. | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |
| L6 | 5117 | (memory same attribut\$3) and configur\$3 and logical | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |
| L7 | 15 | (FPGA or (programmable adj logic adj design) same implement\$5) and (memory same attribut\$3) and configur\$3 and logical and interconnect\$3 and topology and component and "716"/\$.ccls. | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |
| L8 | 30156 | memory same attribut\$3 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |

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| L9 | 2 | "20030033374" | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:13 |
| L10 | 202 | (memory same component same attribut\$3) and interface and implement\$6 and specification and topology and interconnect\$4 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |
| L11 | 171 | (memory same component same attribut\$3) and interface and implement\$6 and specification and topology and interconnect\$4 and messag\$3 and generat\$3 and configur\$4 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |
| L12 | 181 | (memory same component same attribut\$3) and interface and implement\$6 and specification and topology and interconnect\$4 and messag\$3 and generat\$3 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |
| L13 | 169 | (memory same component same attribut\$3) and interface and implement\$6 and specification and topology and interconnect\$4 and messag\$3 and generat\$3 and configur\$4 and logic\$4 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |
| L14 | 1875 | (memory same component same attribut\$3) and interface | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |
| L15 | 31030 | FPGA or (programmable adj logic adj design) same implement\$5 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |
| L16 | 1019 | (memory same component same attribut\$3) and interface and implement\$6 and specification | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |

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| L17 | 231 | (memory same component same attribut\$3) and interface and implement\$6 and specification and topology | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |
| L18 | 94 | (FPGA or (programmable adj logic adj design) same implement\$5) and (memory same attribut\$3) and configur\$3 and logical and interconnect\$3 and topology and component and architecture | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |
| L19 | 326 | (FPGA or (programmable adj logic adj design) same implement\$5) and (memory same attribut\$3) and configur\$3 and logical and interconnect\$3 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |
| L20 | 2 | "20030003374" | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |
| L21 | 2563 | memory same component same attribut\$3 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |
| L22 | 105 | (FPGA or (programmable adj logic adj design) same implement\$5) and (memory same attribut\$3) and configur\$3 and logical and interconnect\$3 and topology | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |
| L23 | 181 | (memory same component same attribut\$3) and interface and implement\$6 and specification and topology and interconnect\$4 and messag\$3 | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:03 |
| L24 | 2 | "20050172085" | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:14 |

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|-----|---|---------------|---|----|----|------------------|
| L25 | 2 | "20050114593" | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:15 |
| L26 | 2 | "20050172085" | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/10/30 06:15 |